Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.009”**

**.015”**

**.009”**

**.008”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size:**

**E = .015 x .008”**

**B = .009”**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .066” X .066” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: 2N5153**

**DG 10.1.2**

#### Rev B, 7/1